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(54) **Semiconductor infrared emitting device with oblique side surface with respect to the cleavage and process of fabrication thereof.**

(57) A semiconductor infrared emitting device is fabricated from an n-type gallium arsenide substrate (11), an n-type gallium arsenide layer (12) on the top surface (11b) of the substrate, a p-type gallium arsenide layer (13) formed on the n-type gallium arsenide layer for forming a p-n junction therebetween, and electrodes (15/ 16) provided on the p-type gallium arsenide layer and the reverse surface of the substrate for applying a bias voltage to the p-n junction, and the side surface (11c) of the substrate declines from the cleavage surface of the gallium arsenide substrate so that the incident angle of infrared varies at the crystal surfaces, thereby allowing the infrared to be radiated from the semiconductor infrared emitting device.

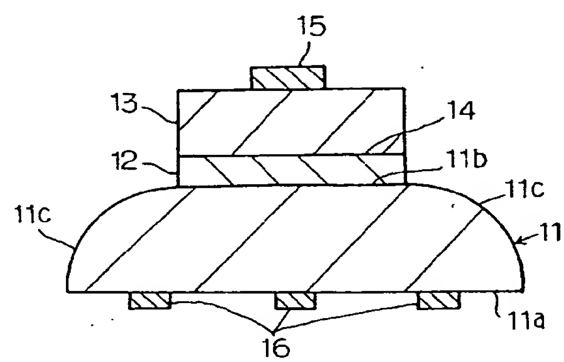

Fig.4

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This invention relates to a semiconductor infrared emitting device and, more particularly, to a structure of a high-power high-efficiency semiconductor infrared emitting device and process of fabricating the structure.

DESCRIPTION OF THE RELATED ART

The semiconductor infrared emitting device finds a wide variety of application such as an indicator incorporated in a remote control system and a part of a photo-coupler, and research and development efforts are made on high efficiency semiconductor infrared emitting device and a simple process sequence for fabrication thereof.

A typical example of the semiconductor infrared emitting device is illustrated in Fig. 1. The prior art semiconductor infrared emitting device is fabricated on an n-type gallium arsenide substrate 1 with orientation of (100), and an n-type gallium arsenide film 2 doped with silicon is grown on the major surface of the n-type gallium arsenide substrate 1. The n-type gallium arsenide film 2 is overlain by a p-type gallium arsenide film 3 also doped with silicon, and an electrode 4 of gold-zinc alloy is patterned on the p-type gallium arsenide film 3. The p-type gallium arsenide film 3 is about 50 microns to 60 microns in thickness. Electrodes 5 of gold-zinc alloy are arranged in dotted pattern on the reverse surface of the gallium arsenide substrate 1, and the dotted pattern aims at enhancement of output efficiency through reflection on the reverse surface.

The prior art semiconductor infrared emitting device is fabricated through a process sequence described hereinbelow. The process sequence starts with preparation of an n-type gallium arsenide wafer serving as the n-type gallium arsenide substrates 1, and the n-type gallium arsenide layer 2 and the p-type gallium arsenide layer are sequentially grown on the n-type gallium arsenide substrate 1 through a single liquid phase epitaxial process. This is because of the fact that silicon is an amphoteric impurity, and such a single epitaxial growth is desirable in view of both cost reduction and high quality. After deposition of gold-zinc alloy, the gold-zinc alloy films are patterned into the electrodes 4 and 5. Finally, the n-type gallium arsenide wafer is separated into the semiconductor infrared emitting devices through a dicing stage, and ach of the semiconductor infrared emitting devices is shaped into a dice.

Fig. 2 illustrates another prior art semiconductor infrared emitting d vice, and the second prior art semiconductor infrared emitting device is similar in structur to the first prior art semiconductor infrared emitting device except for a separation stage from the gallium arsenide wafer. For this reason, films and the first prior art semiconductor infrared emitting device.

The fabrication process for the second semiconductor infrared emitting device traces the epitaxial growing stag , the deposition stage and the patterning stage of the process sequence for the first semiconductor infrared emitting device. However, the orientation flat of the wafer or the direction of cleavage is taken into account of, and the electrodes 4 are elongated in parallel thereto. The separation stage is different from that of the first prior art semiconductor infrared emitting device. Namely, while dicing the gallium arsenide wafer, the gallium arsenide wafer is partially cut, and the individual semiconductor infrared emitting devices are still contiguous to one another through a half or a third of the thickness. After the dicing stage, a roller travels over the reverse surface of the gallium arsenide wafer for breaking into the individual semiconductor infrared emitting devices. Reference numeral 6 designates the cleavage surfaces which take place after the separation through the rolling stage. The cleavage surfaces are of the mirror surface.

However, a problem is encountered in the prior art semiconductor infrared emitting devices in low luminous efficiency. One of the reasons for the low luminous efficiency is the single epitaxial growing stage for both n-type and p-type gallium arsenide layers 2 and 3. The single epitaxial growth is desirable for excellent lattice structure at the p-n junction and the cost saving. However, single epitaxial growth stage can not independently control the dopant concentrations of the gallium arsenide layers 2 and 3. For this reason, the prior art process sequences focuses the optimum dopant concentration upon the p-n junction between the n-type gallium arsenide layer 2 and the p-type gallium arsenide layer 3. If the dopant concentration at the p-n junction is optimized, the p-type gallium arsenide layer 3 has the dopant concentration around 10^{19} cm^{-3}, and the peak wavelength of the infrared ranges between 940 nanometers to 950 nanometers. However, the absorption coefficient is not less than 100 cm^{-1} with respect to the core of the wavelength, and almost half of the infrared is absorbed in the p-type gallium arsenide layer 3 of 50 to 60 microns thick. Additionally, the n-type gallium arsenide layer 2 has the absorption coefficient ranging between 10 cm^{-1} to 20 cm^{-1}.

Another reason for the low luminous efficiency is the reflective index of gallium arsenide. The refractive index of the gallium arsenide is about 3.6, and the critical angle is only 17 degrees. Moreover, the dice-shaped prior art semiconductor infrared emitting devices tends to keep the regularity of incidental angle and reflection angle. For this reason, the infrared IR1 produced in the vicinity of the p-n junction 7 repeats

reflection as shown in Fig. 3, and most of the infrared IR1 is absorbed by the p-type gallium arsenide layer 3 with the large absorption coefficient.

In order to enhance the luminous efficiency, another prior art semiconductor infrared emitting device has a p-type aluminum gallium arsenide layer on the p-type gallium arsenide layer 3. However, the p-type aluminum gallium arsenide layer is not so effective for the high luminous efficiency, and fairly increases the production cost. Therefore, the third prior art semiconductor infrared emitting device is less attractive.

SUMMARY OF THE INVENTION

It is therefore an important object of the present invention to provide a semiconductor infrared emitting device which achieves high luminous efficiency without sacrifice of production cost.

It is another important object of the present invention to provide a process for fabricating the semiconductor infrared emitting device.

To accomplish the object, the present invention proposes to form a side surface of a substrate obliquely extending with respect to a cleavage surface.

In one aspect the invention provides a semiconductor infrared emitting device comprising:

a) a substrate formed of a compound semiconductor and having a side surface; and

b) a multi-layer structure formed on said substrate, and operative to produce infrared when a bias voltage is applied,

characterised in that

said side surface of said substrate extends obliquely with respect to a side surface of said multi-layer structure.

In accordance with another aspect of the present invention, there is provided a semiconductor infrared emitting device comprising:

a) a substrate of one conductivity type formed of first compound semiconductor and from a wafer with a vertical cleavage surface, and having a reverse surface, a top surface substantially parallel to the reverse surface and side surfaces declining from the vertical cleavage surface at a predetermined angle;

b) a first film of the one conductivity type formed of second compound semiconductor, and provided on the top surface of the substrate;

c) a second film of the opposite conductivity type formed of third compound semiconductor, and provided on the first film for forming a p-n junction therebetween;

d) a first electrode formed on the second film; and

e) a second electrode formed on the reverse surface of the substrate.

The invention also provides a process for fabricating a semiconductor infrared emitting device comprising:

a) forming a substrate of a first compound semiconductor;

b) forming a multi-layer structure on said substrate and operative to produce infrared when a bias voltage is applied thereto; and

c) forming a side surface of said substrate which extends obliquely with respect to a side surface of said multi-layer structure.

Another aspect of the invention provides a process of fabricating a semiconductor infrared emitting device comprising the steps of:

a) preparing a wafer of first compound semiconductor having one conductivity type and a vertical cleavage surface;

b) successively growing a first film of said one conductivity type and a second film of the opposite conductivity type on a major surface of said wafer so that said major surface of said wafer is covered with said first film which in turn is overlain by said second film, said wafer, said first film and said second film forming in combination a multi-layer having a p-n junction therebetween;

c) forming electrodes on a top surface of said second film and on a reverse surface of said substrate; and

characterised by

d) forming side surfaces of the substrate so that they extend obliquely relative to said mutual cleavage surface.

In accordance with a further aspect of the present invention, there is provided a process of fabricating a semiconductor infrared emitting device comprising the steps of:

a) preparing a wafer of first compound semiconductor having one conductivity type and a vertical cleavage surface;

b) successively growing a first film of the one conductivity type and a second film of the opposite conductivity type on a major surface of the wafer through a liquid phase epitaxial technique using liquid second compound semiconductor doped with amphoteric impurity atoms so that the major surface of the wafer is covered with the first film which in turn is overlain by the second film, the wafer, the first film and the second film forming in combination a multi-layer structure;

c) forming electrodes on a top surface of the second film and on a reverse surface of the substrate;

d) forming a shallow and wide moat inwardly projecting from the top surface the second film and defined by respective inner walls; e) forming a deep and narrow moat inwardly projecting from the bottom surfaces of the inner walls, respectively, so as to be nested within the shallow and wide moat; f) repeating the step e) in such a manner as to nest a deeper and narrower moat g) sep-

arating the multi-layer structure into a plurality of semiconductor infrared emitting devices along the deepest and narrowest moat.

In accordance with yet another aspect of the present invention, there is provided a process of fabricating a semiconductor infrared emitting device comprising the steps of: a) preparing a wafer of first compound semiconductor having one conductivity type and an orientation flat surface; b) successively growing a first film of the one conductivity type and a second film of the opposite conductivity type on a major surface of the wafer through a liquid phase epitaxial technique using liquid second compound semiconductor doped with amphoteric impurity atoms so that the major surface of the wafer is covered with the first film which in turn is overlain by the second film, the wafer, the first film and the second film forming in combination a multi-layer structure; c) forming upper electrodes and lower electrodes on a top surface of said second film and on a reverse surface of said wafer, said upper electrodes being arranged in rows and columns, said rows of upper electrodes obliquely extending with respect to said orientation flat surface at a predetermined angle; d) forming a moat inwardly projecting from the top surface the second film in such a manner as to pass between the rows of upper el ctrodes; and e) separating the multi-layer structure into a plurality of semiconductor infrared emitting d vices along the moat.

BRIEF DESCRIPTION OF THE DRAWINGS

The feature and advantages of the semiconductor infrared emitting device and the process of fabrication thereof according to the present invention will b more clearly understood from the following description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a cross sectional view showing the structure of the first prior art semiconductor infrared emitting device;

Fig. 2 is a cross sectional view showing the structure of the second prior art semiconductor infrared emitting device;

Fig. 3 is a view showing the multiple reflection of the infrared in the prior art semiconductor infrared emitting device;

Fig. 4 is a cross sectional view showing the structure of a semiconductor infrared emitting device according to the present invention;

Fig. 5 is a view showing the multiple reflection of the infrared produced in the semiconductor infrared emitting device;

Fig. 6 is a graph showing the amount of infrared in terms of forward bias current supplied to the semiconductor infrared emitting device shown in Fig. 4;

Figs. 7A to 7D are cross sectional views showing a process sequence for fabricating the semiconductor infrared emitting device shown in Fig. 5;

Figs. 8A and 8B are cross sectional views showing a part of another process sequence for fabricating the semiconductor infrared emitting device;

Fig. 9 is a cross sectional view showing the structure of another semiconductor infrared emitting device according to the present invention;

Fig. 10 is a view showing the multiple reflection of the infrared produced in the semiconductor infrared emitting device shown in Fig. 9;

Fig. 11 is a graph showing the amount of infrared in terms of forward bias current supplied to the semiconductor infrared emitting device shown in Fig. 9;

Figs. 12A to 12D are cross sectional views showing a process sequence for fabricating the semiconductor infrared emitting device shown in Fig. 9; and

Fig. 13 is a plane view showing the arrangement of upper electrodes in the process sequence shown in Figs. 12A to 12D.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

Referring to Fig. 4 of the drawings, a semiconductor infrared emitting device embodying the present invention is fabricated on an n-type gallium arsenide substrate 11 with orientation of (100), and the n-type gallium arsenide substrate 11 is shaped into a generally frusto-conical configuration. Namely, the n-type gallium arsenide substrate 11 has a reverse surface 11a larger in area than a major surface 11b thereof, and a curved side surface 11c is merged thereinto like a flared skirt. The curved side surface 11c is one and half times larger in area than the side surface of the first prior art semiconductor infrared emitting device. An n-type gallium arsenide layer 12 is formed on the major surface 11b, and is overlain by a p-type gallium arsenide layer 13. Both n-type and p-type gallium arsenide layers 12 and 13 are doped with silicon, and a p-n junction 14 is formed along the boundary between the n-type gallium arsenide layer 12 and the p-type gallium arsenide layer 13. The oblique side surface 11c is wider than a vertical surface merged into a major surface and a reverse surface of a cubic substrate, and such an oblique side surface 11c is desirable for the infrared emitting device, because the area of the side surface 11c is one point seven times larger than that of the prior art.

An electrode 15 of gold-zinc alloy is formed on the p-type gallium arsenide layer 13, and other electrodes 16 of gold-germanium are formed on the reverse surface 11a in a dotted pattern.

The semiconductor infrared emitting device thus arranged behave as follows. If an appropriate bias voltage is applied between the electrode 15 and the electrodes 16, infrared IR2 is generated around the p-n junction. The infrared IR2 is assumed to upwardly and rightwardly proceed from a point 14a. The infrared IR2 is multiply reflected and traces a path indicated by arrows AR1. However, the infrared IR2 is taken out from the semiconductor infrared emitting device after three total reflections at 14b, 14c and 14d. Although the first prior art semiconductor infrared device absorbs the infrared IR1 after the five total reflections, the frusto-conical gallium arsenide substrate 11 effectively takes out the infrared IR2, and, accordingly, enhances the luminous efficiency. In detail, if a semiconductor infrared emitting device is shaped into a rectangular parallelopiped configuration such as a cube, the incident angles is theoretically equal at every crystal boundary, and infrared repeats the total reflection. This results in that most of the infrared IR1 is absorbed without radiating therefrom due to the large absorption coefficient of gallium arsenide. However, if the side surface of a semiconductor infrared emitting device obliquely extends with respect to either bottom or top surface, the incident angle onto the crystal boundaries is variable, and the infrared IR2 is much liable to be taken out from the semiconductor infrared emitting device.

Thus, the oblique side surface 11c to the crystal boundary allows the infrared to be taken out from the semiconductor infrared emitting device. The side surface 11c is larger in area than a virtual surface parallel to the cleavage surface 17 in so far as one of the peripheries of the upper and reverse surfaces 11b and 11a is larger than the other of the peripheries. In other words, the side surface 11c contains an area declining from the cleavege surface 17 at greater than zero degrees or less than 90 degrees, the side surface 11c is effective against the absorption, and the amount of the infrared IR2 taken out therefrom is effectively increased. The area may decline from the cleavege surface at an angle greater than -90 degrees and less than zero. Moreover, it is desirable for the area of the side surface 11c to decline from the cleavege surface 17 at an angle ranging from 5 degrees to 85 degrees. Of course, an area ranging from -85 degrees and -5 degrees is also effective.

In order to make the difference from the first prior art semiconductor infrared emitting device shown in Fig. 3 clear, the amount of the infrared IR1 and the amount of the infrared IR2 were measured. An appropriate infrared-detector (not shown) was faced to the semiconductor infrared emitting device according to the present invention, the infrared-detector converted the infrared IR2 radiated therefrom into current, and the amount of current was proportional to the amount of infrared. While the forward bias voltage was increased from zero to 100 milliamperes, the amount of current or the amount of the infrared IR2 traced plots PT1 as shown in Fig. 6. On the other hand, while the forward bias current to the first prior art semiconductor infrared emitting device was similarly increased, the infrared detector increased the amount of current as shown in plots PT2. Comparing the plots PT1 with the plots PT2, the amount of the infrared IR2 is one and half times larger than the amount of the infrared IR1.

The semiconductor infrared emitting device shown in Fig. 4 is fabricated through a process sequence, and description is hereinbefore made on the process sequence with reference to Figs. 7A to 7D.

The process sequence starts with preparation of an n-type gallium arsenide wafer 21 having orientation of (100). An n-type gallium arsenide layer 22 and a p-type gallium arsenide layer 23 are successively grown through a liquid-phase slow-cooling epitaxial technique using liquid gallium arsenide doped with silicon. The silicon is one of amphoteric impurities, and serves as donor impurities for the n-type gallium arsenide layer 22 and as acceptor impurities for the p-type gallium arsenide layer 23. The resultant multilayer structure of this stage is illustrated in Fig. 7A.

Subsequently, gold-zinc alloy is selectively grown on the top surface of the p-type gallium arsenide layer through an appropriate mask, and gold-germanium alloy is also selectively grown on the reverse surface of the n-type gallium arsenide wafer 21 through another appropriate mask. Pieces of gold-zinc alloy serve as the upper electrodes 15, and pieces of gold-germanium alloy serve as the lower electrodes 16. In this instance, the upper electrodes 15 are arranged in rows and columns, and the rows of upper electrodes 15 The resultant multi-layer structure of this stage is illustrated in Fig. 7B.

A shallow and wide moat 24a is formed in th multilayer structure, and project from the top surface of the p-type gallium arsenide layer 23 into the n-type gallium arsenide wafer 21 through a dicing technique. Subsequently, a deep and narrow moat 24b is formed in the n-type gallium arsenide wafer 21, and project from the bottom surfaces partially defining the shallow and wide moat also through a dicing technique. The deep and narrow moat 24b is nested within the shallow and wide moat 24a. The dicing stage is repeated for forming a deep and narrow moat 24c, and the moat 24c is nested within the moat 24b. Then, a deeper and narrower moat is nested within a shallower and wider moat, and the multiple moat structure 24 extends between a plurality of semiconductor infrared emitting devices arranged in rows and columns, and separates the n-type and p-type gallium arsenide layers 12 and 13 of a semiconductor infrared emitting device from the n-type and p-type gallium arsenide layers 12 and 13 of another semiconductor infrared emitting device as shown in Fig. 7C.

An adhesive flexible film 25 is bonded to the re-

verse surface of the n-type gallium arsenide wafer 21, and a roller 26 exerts force on the n-type gallium arsenide substrate 21. Then, the n-type gallium arsenide wafer 21 is broken into the n-type gallium arsenide substrates 11, and the n-type gallium arsenide substrates 11 are shaped into generally frusto-conical configuration.

The process sequence described hereinbefore forms the multiple moat structure 24 through dicing stages. However, a lithographic technique followed by an etching stage is available for the multiple moat structure 24. Namely, after the formation of the upper and lower electrodes 15 and 16, a photoresist mask 27a is patterned on the p-type gallium arsenide layer 23 through the lithographic technique, and the p-type gallium arsenide layer 23, the n-type gallium arsenide layer 22 and the n-type gallium arsenide substrate 21 are partially removed by using an appropriate etchant. Then, the shallow and wide moat 24a takes place in the multi-layer structure as shown in Fig. 8A. The lithographic technique and the etching are repeated, and a photoresist mask 27b allows the etchant to form the deep and narrow moat 24c as shown in Fig. 8B. The moats 24a, 24b and 24c are sequentially nested with one another, and the multiple moat structure 24 is formed through the lithographic technique followed by the etching. After the formation of the multiple moat structure, the multi-layer structure is separated into a plurality of semiconductor infrared emitting devices as similar to that shown in Fig. 7D.

Second Embodiment

Turning to Fig. 9 of the drawings, another semiconductor infrared emitting device embodying the present invention is fabricated on an n-type gallium arsenide substrate 31 with orientation of (100), and the n-type gallium arsenide substrate 11 has a reverse surface 31a, a major surface 31b substantially parallel to the reverse surface 31a, and side surfaces 31c and 31d extending in parallel to each other and declining from the reverse surface 31a.

An n-type gallium arsenide layer 32 is formed on the major surface 31b, and is overlain by a p-type gallium arsenide layer 33. Both n-type and p-type gallium arsenide layers 12 and 13 are doped with silicon, and a p-n junction 34 is formed along the boundary between the n-type gallium arsenide layer 32 and the p-type gallium arsenide layer 33.

An upper electrode 35 of gold-zinc alloy is formed on the p-type gallium arsenide layer 33, and lower electrodes 36 of gold-germanium alloy are formed on the reverse surface 31a in a dotted pattern.

As will be described hereinlater, the side surfaces 31c and 31d decline from the cleavage surface CLV of an n-type gallium arsenide wafer with orientation of (100), and the angle AG between the cleavage surface CLV and the side surface 31d is regulated to an angle greater than -90 degrees and less than 90 degrees. Since the oblique side surfaces 31c and 31d are larger in area than a vertical side surface such as the vertical side surface of 6 of the prior art structure shown in Fig. 2, the semiconductor infrared emitting device shown in Fig. 9 allows the infrared produced therein to be radiated at higher probability, and, accordingly, is improved in luminous efficiency. If the side surface 31d ranges from 5 degrees to 85 degrees or -85 degrees to -5 degrees, the luminous efficiency is effectively increased.

The semiconductor infrared emitting device thus arranged behave as follows. If an appropriate bias voltage is applied between the electrode 35 and the electrodes 36, infrared IR3 is generated around the p-n junction 34. The infrared IR3 is assumed to upwardly and rightwardly proceed from a point 34a. The infrared IR3 is multiply reflected and traces a path indicated by arrows AR2. However, the infrared IR3 is taken out from the semiconductor infrared emitting device after three total reflections at 34b, 34c and 34d. Although the first prior art semiconductor infrared device absorbs the infrared IR1 after the five total reflections, the arsenide substrate 31 effectively takes out the infrared IR3, and, accordingly, enhances the luminous efficiency. This is because of the fact that the total surface area of the n-type gallium arsenide substrate 31 is increased than a cubic shaped substrate.

In order to make the difference from the first prior art semiconductor infrared emitting device shown in Fig. 3 clear, the amount of the infrared IR3 was measured as similar to the first embodiment. Namely, an appropriate infrared-detector (not shown) was faced to the semiconductor infrared emitting device shown in Fig. 9, the infrared-detector converted the infrared IR3 radiated therefrom into current, and the amount of current was proportional to the amount of infrared. While the forward bias voltage was increased from zero to 100 milliamperes, the amount of current or the amount of the infrared IR3 traced plots PT3 as shown in Fig. 11. The amount of the infrared IR1 is also plotted in Fig. 11, and the plots PT1 stands for the amount of infrared produced in not only the first prior art semiconductor infrared emitting device shown in Fig. 1 but also the second prior art semiconductor infrared emitting device shown in Fig. 2. Comparing the plots PT1 with the plots PT3, the amount of the infrared IR3 is one point three times larger than the amount of the infrared IR1. The second embodiment is less effective rather than the first embodiment in view of the luminous efficiency. However, the fabrication process for the second embodiment is simpler than that of the first embodiment as described hereinbelow, and is desirable in view of productivity.

The semiconductor infrared emitting device shown in Fig. 9 is fabricated through a process sequence, and description is hereinbefore made on the

process sequence with reference to Figs. 12A to 12D.

The process sequence starts with preparation of an n-type gallium arsenide wafer 41 having orientation of (100). The orientation flat surface is labeled with "OF" in Fig. 13, and is substantially vertical to the reverse surface of the n-type gallium arsenide wafer 41. An n-type gallium arsenide layer 42 and a p-type gallium arsenide layer 43 are successively grown through a liquid-phase slow-cooling epitaxial technique using liquid gallium arsenide doped with silicon. The silicon is one of amphoteric impurities, and serves as donor impurities for the n-type gallium arsenide layer 42 and as acceptor impurities for the p-type gallium arsenide layer 43. The resultant multi-layer structure of this stage is illustrated in Fig. 12A.

Subsequently, gold-zinc alloy is selectively grown on the top surface of the p-type gallium arsenide layer, and gold-germanium alloy is also selectively grown on the reverse surface of the n-type gallium arsenide wafer 41. The upper electrodes 35 and the lower electrodes 36 are formed from the gold-zinc alloy film and the gold-germanium alloy film on the top surface of the p-type gallium arsenide layer 43 and the reverse surface of the n-type gallium arsenide wafer 41. The upper electrodes 35 are arranged in rows and columns so as to form an array 44 as shown in Fig. 13, and the rows of upper electrodes decline from the orientation flat surface OF at 10 degrees. However, the angle AGL between the rows and the orientation flat surface OF may range from 5 degrees to 85 degrees.

Grooves are formed in the multi-layer structure by using a dicing technique, and real lines 45a and 45b are indicative of the longitudinal directions of the grooves. The grooves 45a extend between the rows of upper electrodes in parallel thereto, and the grooves 45b cross the grooves 45a at right angle as will be seen from Fig. 13. The grooves 45a and 45b are as deep as a half of the total thickness of the multi-layer structure. The resultant multi-layer structure is illustrated in Fig. 12C.

An adhesive flexible film 46 is bonded to the reverse surface of the n-type gallium arsenide wafer 21, and a roller 47 travels along the grooves 45a and 45b. Force is exerted on the n-type gallium arsenide substrate 41. Then, cracks 48 take place from the grooves to the reverse surface of the wafer 41, and the n-type gallium arsenide wafer 41 is broken into the n-type gallium arsenide substrates 31. The cracks 48 are oblique due to the grooves 45a obliquely extending with respect to the orientation flat surface OF, and the side surfaces of the substrates 31 decline from the cleavage surface.

Although particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the present invention. For example, compound semiconductor is not limited to gallium arsenide, and an etchant may be applied to the multiple moat structure formed through the dicing stages for creating smooth surfaces.

Claims

1. A semiconductor infrared emitting device comprising:
   a) a substrate (11; 31) formed of a compound semiconductor and having a side surface; and
   b) a multi-layer structure (12/13; 32/33) formed on said substrate, and operative to produce infrared when a bias voltage is applied,

   characterised in that
   said side surface (11c; 31c/31d) of said substrate extends obliquely with respect to a side surface of said multi-layer structure.

2. A semiconductor infrared emitting device comprising:
   a) a substrate (11;31) of one conductivity type formed of first compound semiconductor and from a wafer with a vertical cleavage surface (17; CLV), and having a reverse surface (11a; 31a), a top surface (11b; 31b) substantially parallel to said reverse surface and side surfaces (11c; 31c/31d);
   b) a first film (12; 32) of said one conductivity type formed of second compound semiconductor, and provided on said top surface of said substrate;
   c) a second film (13; 33) of the opposite conductivity type formed of third compound semiconductor, and provided on said first film for forming a p-n junction therebetween (14;34);
   d) a first electrode (15; 35) formed on said second film; and
   e) a second electrode (16; 36) formed on said reverse surface of said substrate,

   characterised in that said side surfaces (11c; 31c/31d) extend obliquely relative to said vertical cleavage surface (17; CLV).

3. A device as set forth in Claim 2, in which said first, second and third compound semiconductors are gallium arsenide.

4. A device as set forth in any preceding claim, in which said side surface or surfaces (11c) are non-flat.

5. A device as set forth in any of Claims 1 to 3, in which said side surface or surfaces are substantially flat.

6. A device as set forth in any preceding claim, in which said side surface or surfaces are curved.

7. A device as set forth in any of Claims 1 to 5, in which said side surface or surfaces of the substrate (11c, 31c/31d) extend obliquely at a predetermined angle, the magnitude of which is greater than zero and less than 90 degrees.

8. A device as set forth in Claim 7, in which the magnitude of said predetermined angle ranges from 5 degrees to 85 degrees.

9. A device as set forth in Claim 8, in which said predetermined angle is approximately 10 degrees.

10. A process for fabricating a semiconductor infrared emitting device comprising:

a) forming a substrate (11, 31) of a first compound semiconductor;

b) forming a multi-layer structure (12/13; 32/33) on said substrate and operative to produce infrared when a bias voltage is applied thereto; and

c) forming a side surface (11c; 31c/31d) of said substrate which extends obliquely with respect to a side surface of said multi-layer structure.

11. A process of fabricating a semiconductor infrared emitting device comprising the steps of:

a) preparing a wafer (21) of first compound semiconductor having one conductivity type and a vertical cleavage surface;

b) successively growing a first film (22) of said one conductivity type and a second film (23) of the opposite conductivity type on a major surface of said wafer so that said major surface of said wafer is covered with said first film which in turn is overlain by said second film, said wafer, said first film and said second film forming in combination a multi-layer having a p-n junction therebetween;

c) forming electrodes (15/16) on a top surface of said second film and on a reverse surface of said substrate; and

characterised by

d) forming side surfaces (11c; 31c/31d) of the substrate so that they extend obliquely relative to said mutual cleavage surface.

12. A process as set forth in Claim 11, wherein the obliquely extending side surfaces are formed by:

a) forming a moat (24) in said multi-layer structure; and

b) separating said multi-layer structure into a plurality of semiconductor infrared emittng devices along said moat (24), said step (b) comprising the sub-steps of:

b-1) forming a shallow and wide sub-moat (24a) inwardly projecting from said top surface said second film and defined by respective inner walls;

b-2) forming a deep and narrow sub-moat (24b) inwardly projecting from the bottom surfaces of said inner walls, respectively, so as to be nested within said shallow and wide sub-moat; and

b-3) repeating said sub-step b-2) in such a manner as to nest a deeper and narrower sub-moat (24c) within a shallower and wider sub-moat (24b), if necessary.

13. A process as set forth in Claim 12, in which said shallow and wide sub-moat and said deep and narrow sub-moat are formed by using a dicing technique.

14. A process as set forth in Claim 12 or 13, in which said shallow and wide sub-moat and said deep and narrow sub-moat are formed by using a lithographic technique followed by an etching.

15. A process as claimed in Claim 11 comprising the steps of:

a) preparing as said substrate a wafer (41) of first compound semiconductor having one conductivity type and an orientation flat surface (OF);

b) successively growing a first film (32) of said one conductivity type and a second film (33) of the opposite conductivity type on a major surface of said wafer so that said major surface of said wafer is covered with said first film which in turn is overlain by said second film, said first film and said second film forming in combination said multi-layer structure;

c) forming upper electrodes (35) and lower electrodes (36) on a top surface of said second film and a reverse surface of said wafer, said upper electrodes being arranged in rows and columns, and extending with respect to said orientation flat surface at a predetermined angle.

d) forming a moat (45a/45b) inwardly projecting from said top surface said second film in such a manner a: to pass between said rows of upper electrodes and between said columns of upper electrodes; and

e) separating said multi-layer structure into a plurality of semiconductor infrared emitting devices along said moat.

16. A process as set forth in Claim 15, in which said predetermined angle ranges from 5 degrees to 85 degrees.

17. A process as set forth in Claim 16, in which said predetermined angle is approximately to 10 degrees.

18. A process as set forth in any of Claims 15 to 17, in which the depth of said moat is about a half of the total thickness of said multi-layer structure.

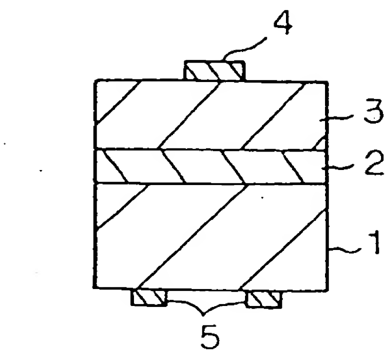


Fig.1
PRIOR ART

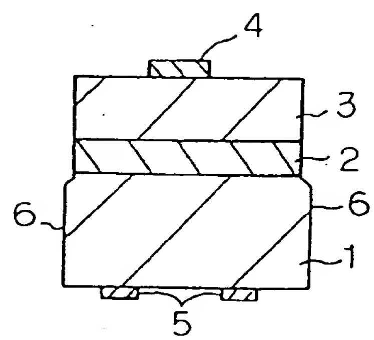


Fig.2
PRIOR ART

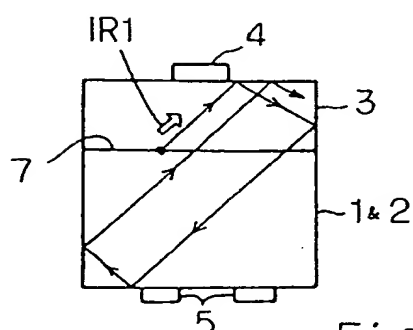


Fig.3
PRIOR ART

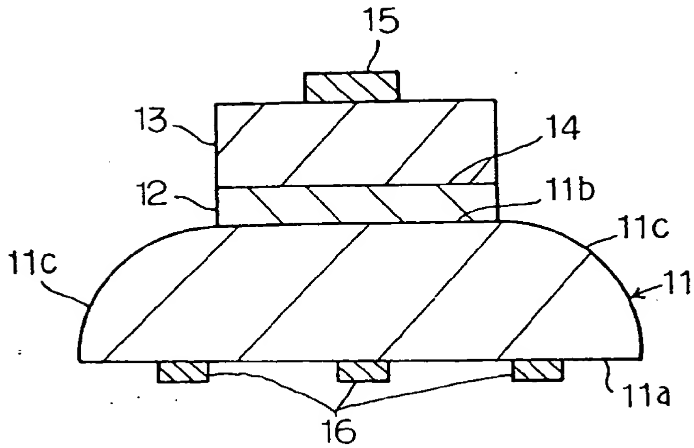

15
13
14
12
11b
11c
11c
11
11a
16

Fig. 4

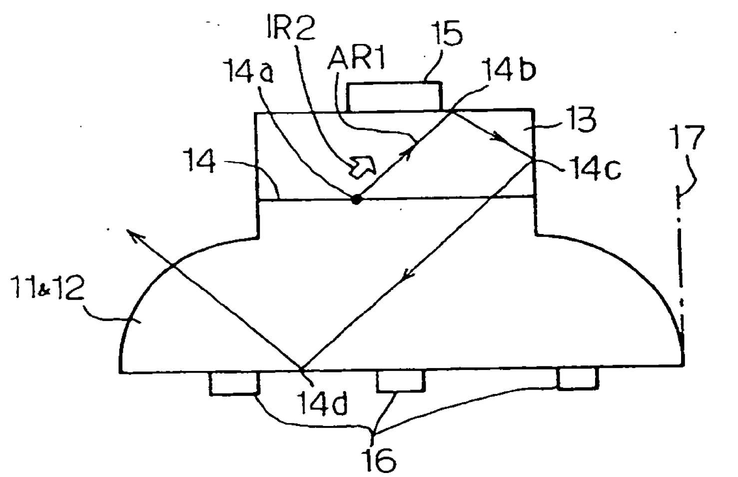

IR2
15
AR1
14a
14b
13
14
14c
17
11&12
14d
16

Fig. 5

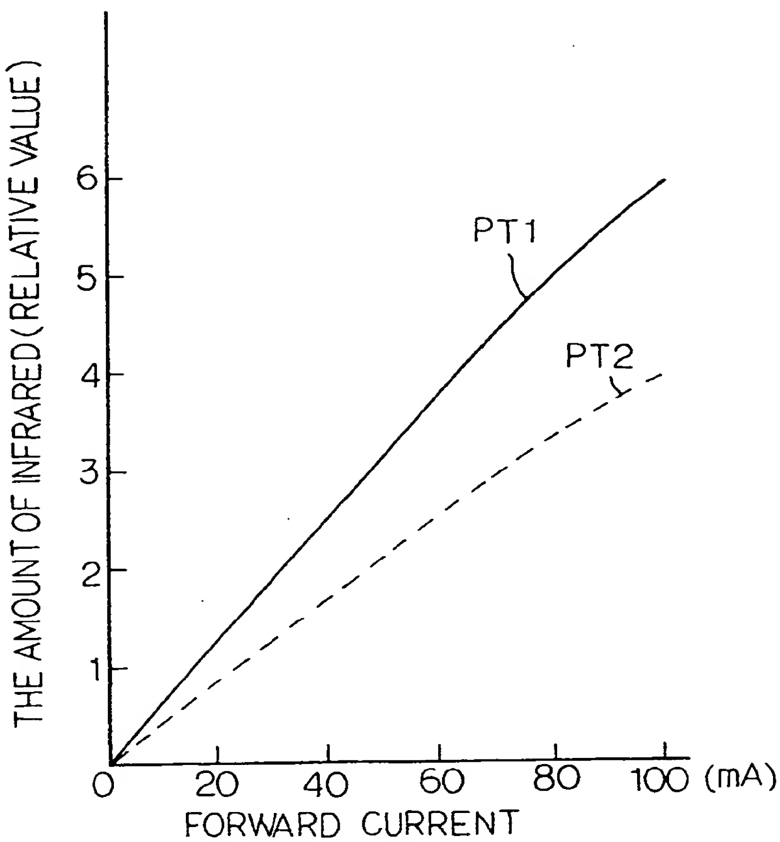

THE AMOUNT OF INFRARED (RELATIVE VALUE)
6
5
4
3
2
1
0
20
40
60
80
100 (mA)
FORWARD CURRENT
PT1
PT2

Fig.6

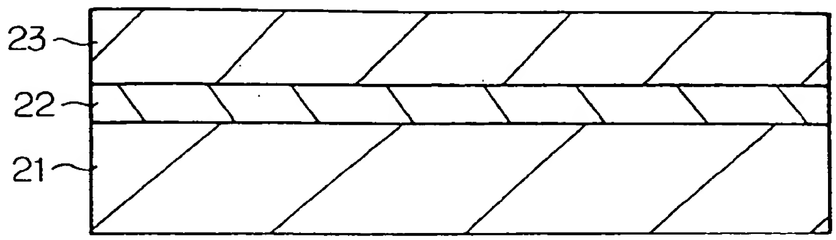


Fig. 7A

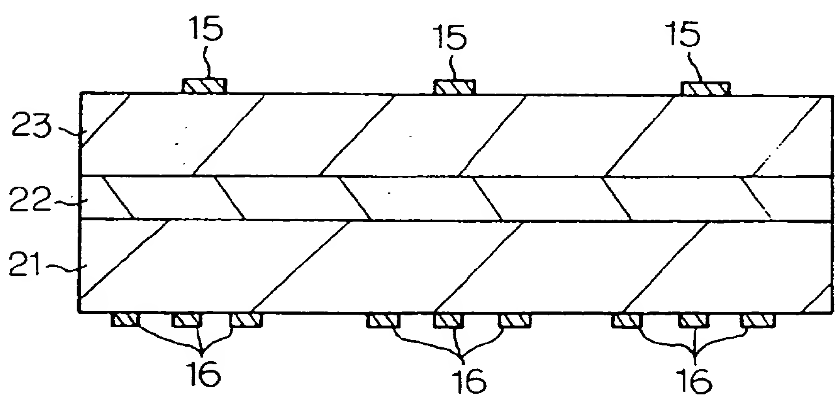
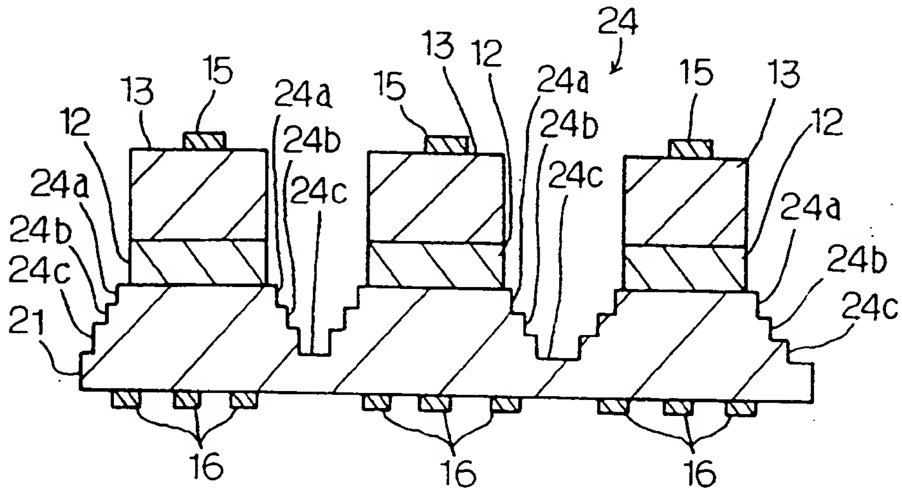
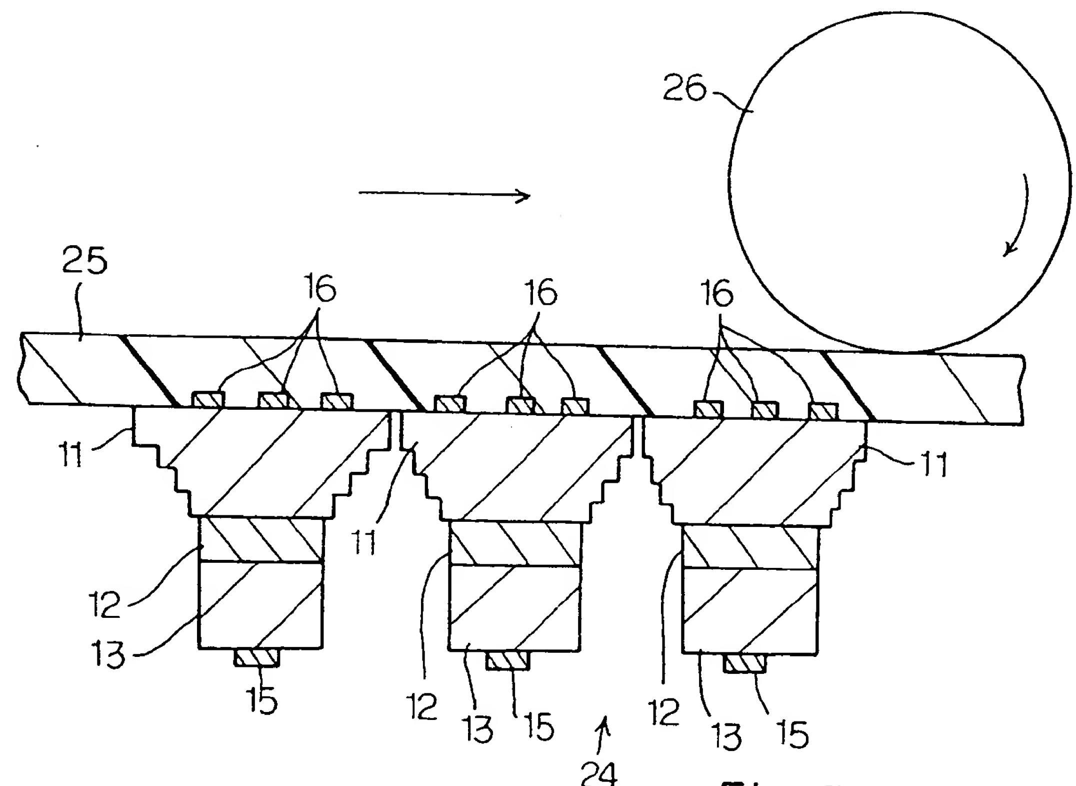


Fig. 7B



Fig·7C



Fig·7D

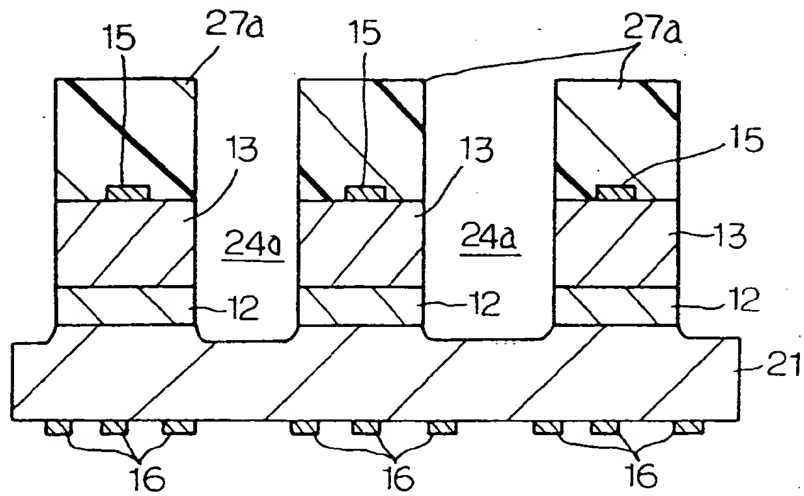

15
27a
15
27a
15
13
13
13
24a
24a
12
12
12
21
16
16
16

Fig. 8A

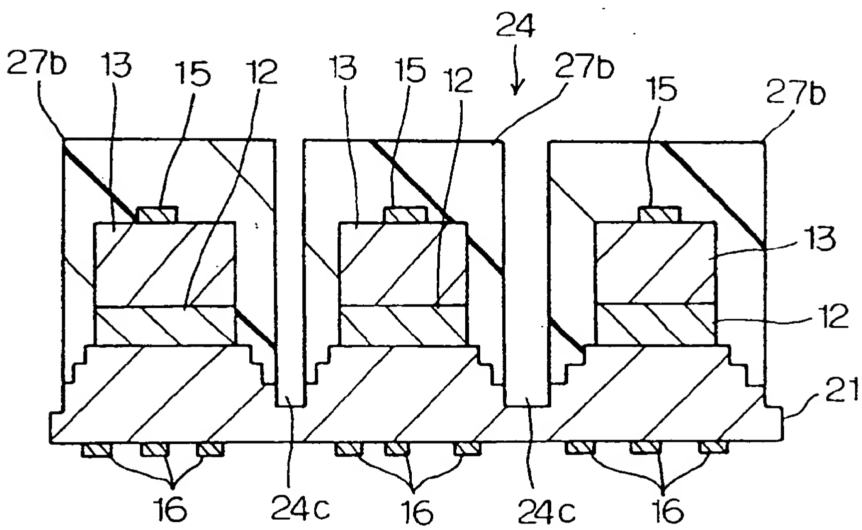

24
27b
13
15
12
13
15
12
27b
15
27b
13
12
21
16
24c
16
24c
16

Fig. 8B

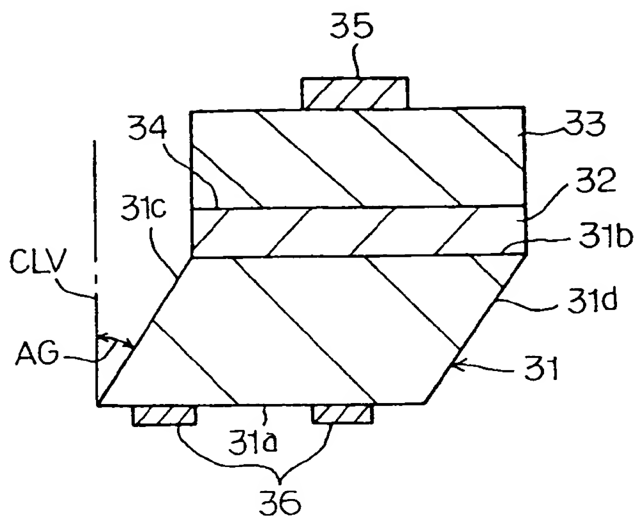

35
34
33
32
31c
31b
CLV
31d
AG
31
31a
36

Fig. 9

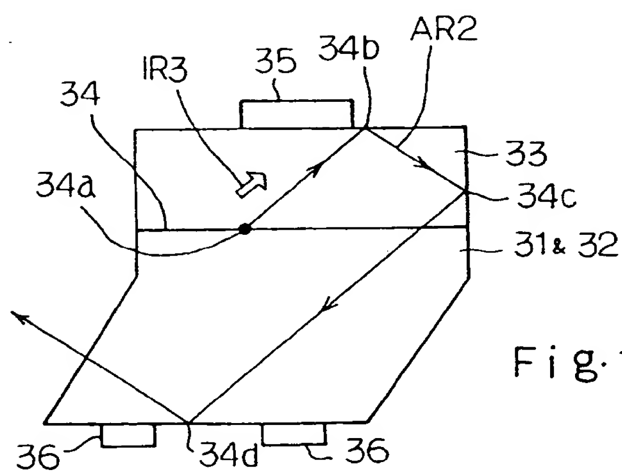
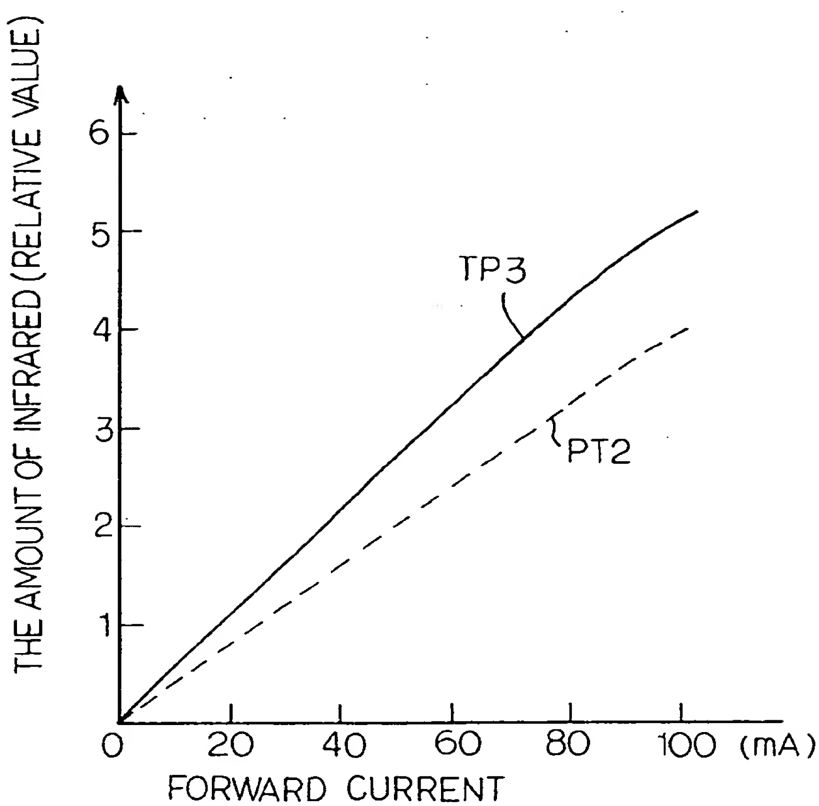

AR2
IR3
35
34b
34
33
34a
34c
31& 32
36
34d
36

Fig. 10


THE AMOUNT OF INFRARED (RELATIVE VALUE)
6
5
4
3
2
1
0
20
40
60
80
100 (mA)
FORWARD CURRENT
TP3
PT2

Fig·11

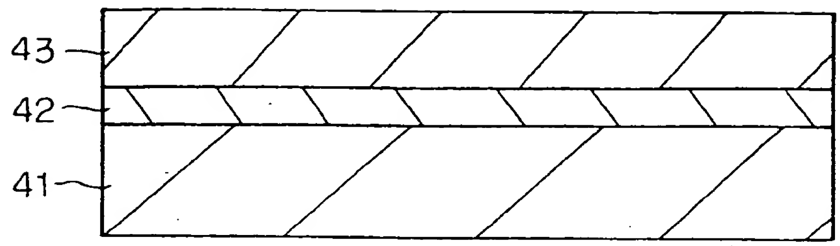


Fig. 12A

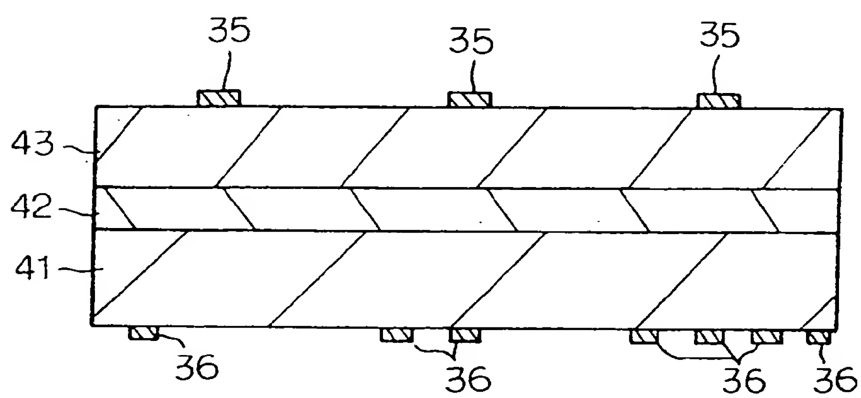


Fig. 12B

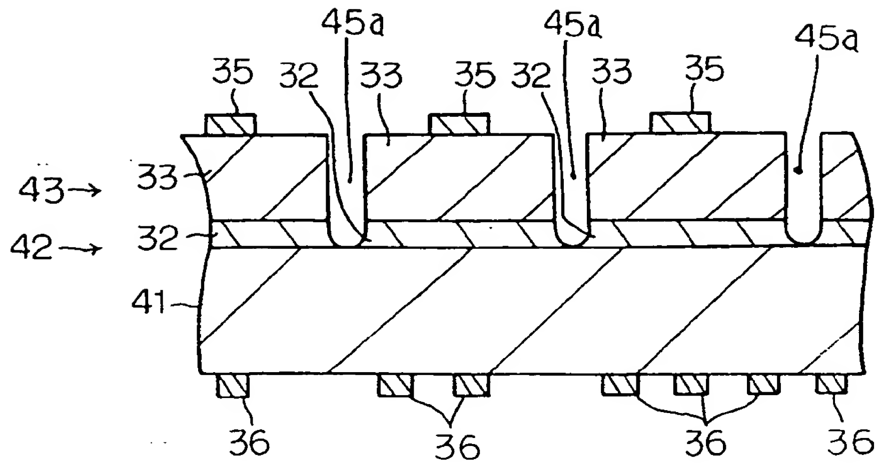


Fig.12C

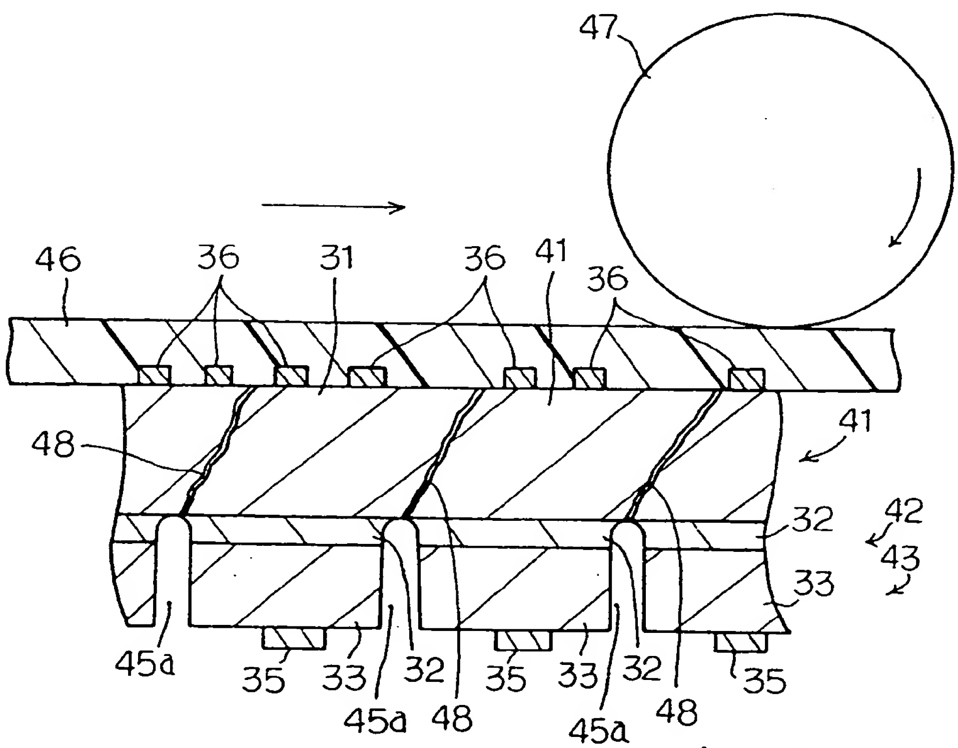


Fig.12D

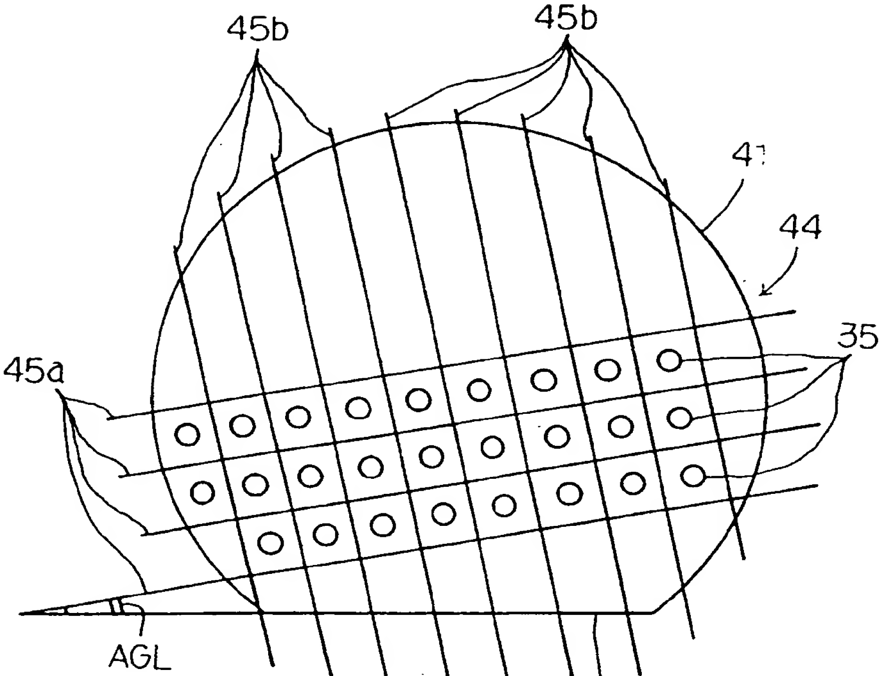


Fig.13

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 93 30 2378

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 405 757 (HEWLETT-PACKARD COMPANY) * page 3, line 5 - line 57 * * page 4, line 53 - page 5, line 4; figures *	1-3,5, 7-10	H01L33/00
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 13 (E-573)14 January 1988 & JP-A-62 173 773 (SHARP CORP) 30 July 1987 * abstract *	1,2,4, 6-8, 10-11	
A	PATENT ABSTRACTS OF JAPAN vol. 7, no. 123 (E-178)(1268) 27 May 1983 & JP-A-58 40 872 (NIPPON DENKI K.K.) 9 March 1983 * abstract *	1,2,4, 6-8	
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 212 (E-339)(1935) 29 August 1985 & JP-A-60 74 642 (NIPPON DENKI K.K.) 26 April 1985 * abstract *	11-13	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L
A	PATENT ABSTRACTS OF JAPAN vol. 11, no. 312 (E-548)12 October 1987 & JP-A-62 105 446 (SHARP CORP) 15 May 1987 * abstract *	11,15-17	
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 243 (E-277)8 November 1984 & JP-A-59 121 830 (MITSUBISHI MONSANTO KASEI KK) 14 July 1984 * abstract *	1-3, 10-11	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	08 JULY 1993	DE LAERE A.L.

CATEGORY OF CITED DOCUMENTS

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E : earlier patent document, but published on, or after the filing date
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& : member of the same patent family, corresponding document

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